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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/580,119	05/30/2000	Leif Magnus Andre Nilsson	040070-666	1475

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EXAMINER
ODOM, CURTIS B

ART UNIT	PAPER NUMBER
2634	3

DATE MAILED: 07/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/580,119	NILSSON ET AL.	
	Examiner	Art Unit	
	Curtis B. Odom	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 May 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 9-12 and 25-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Sumi (U.S. Patent No. 5, 729, 179).

Regarding claim 9, Sumi discloses a PLL (Fig. 30) comprising:

a phase detector (Fig. 30, blocks 152 and 153, column 22, lines 52-60) that has a reference signal input that receives a reference clock signal and a comparison signal input that receives a comparison signal, wherein the phase detector generates a phase difference signal that represents a phase difference between the reference signal and a signal having twice the frequency of the comparison signal;

a circuit (Fig. 30, block 142, column 22, lines 34-36 and 61-64) that generates a PLL output signal having a frequency that is a function of the phase difference signal;

a frequency divider (Fig. 30, block 141, column 22, lines 34-36) that receives the PLL output signal and generates therefrom a divided frequency signal; and

a circuit (Fig. 30, block 149, column 22, lines 41-51 and column 23, lines 3-8) that generates the comparison signal from the divided frequency signal, wherein the comparison signal has one half the frequency of the divided frequency signal, wherein the comparison signal contains only one half (odd or even pulses) the frequency of the divided frequency signal.

Regarding claim 10, which inherits the limitations of claim 9, Sumi discloses the circuit that generates the comparison signal is a latch device configured to toggle a latch device output state once for each cycle of the divided frequency signal (Fig. 30, block 149, column 22, lines 41-51 and column 23, lines 3-8).

Regarding claim 11, which inherits the limitations of claim 10, Sumi discloses the latch device is configured to toggle the latch device output state once for each leading edge of the divided frequency signal (Fig. 30, block 149, column 22, lines 41-51 and column 23, lines 3-8).

Regarding claim 12, which inherits the limitations of claim 10, Sumi discloses the latch device is configured to toggle the latch device output state once for each trailing edge of the divided frequency signal (Fig. 30, block 149, column 22, lines 41-51 and column 23, lines 3-8).

Regarding claims 25-28, the claimed method includes features that correspond with subject matter mentioned above in the rejection of claims 9-12 is applicable hereto.

3. Claims 1-8 and 21-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Lindquist et al. (U.S. Patent 6, 198, 355).

Regarding claim 1, Lindquist et al. discloses a phase detector (Fig. 2), comprising:

a first input (Fig. 2, element 2, column 3, lines 17-27) that receives a reference clock signal;

a second input (Fig. 2, element 14, column 3, lines 17-27) that receives a comparison signal; and

a comparison circuit (Fig. 2, column 3, lines 33-67) that compares a phase of the reference clock signal with a phase of a signal having a frequency that is twice that of the comparison signal.

Regarding claim 2, which inherits the limitations of claim 1, Lindquist et al. discloses the comparison circuit comprises:

a first circuit (Fig. 2, block 32, column 3, lines 46-52) that asserts a first signal having a predetermined logic level in response to only one of a leading edge and a trailing edge of the reference clock signal; and

a second circuit (Fig. 2, blocks 28 and 30, column 3, lines 33-46) that asserts a second signal having a predetermined logic level in response to either one of a leading edge and a trailing edge of the reference clock signal.

Regarding claim 3, which inherits the limitations of claim 2, Lindquist et al. discloses the comparison circuit further comprises:

a reset circuit (Fig. 2, blocks 44 and 46, column 3, lines 58-61) that generates reset signal that resets both the first circuits and the second circuit in response to both the first signal and the second signal being asserted.

Regarding claim 4, which inherits the limitations of claim 3, Lindquist et al. discloses the reset circuit comprises a delay circuit that delays generation of the reset signal for a predetermined length of time after both the first and second signal are asserted (Fig. 2, block 46, column 3, lines 58-61).

Regarding claim 5, which inherits the limitations of claim 2, Lindquist et al. discloses the second circuit is a dual-edge triggered latch (column 1, lines 56-58 and column 3, lines 33-46).

Regarding claim 6, which inherits the limitations of claim 5, Lindquist et al. discloses the dual-edge triggered latch comprises:

a first latch device (Fig. 2, blocks 28, column 3, lines 33-46) coupled to receive the comparison signal in a way such that the first latch device generates a first latch output signal having a predetermined logic level in response to a leading edge of the comparison signal, wherein the latch device would perform the operation on the comparison signal in the same manner as it performs the operation on the reference signal in the present invention;

a second latch device (Fig. 2, blocks 30, column 3, lines 33-46) coupled to receive the comparison signal in a way such that the second latch device generates a second latch output signal having a predetermined logic level in response to a trailing edge of the comparison signal, wherein the latch device would perform the operation on the comparison signal in the same manner as it performs the operation on the reference signal in the present invention; and

a combining logic circuit (Fig. 2, block 36, column 3, lines 44-46) that generates the second signal by combining the first latch output signal and the second latch output signal.

Regarding claim 7, which inherits the limitations of claim 6, Lindquist et al. discloses the combining logic circuit is a logical OR gate (Fig. 2, block 36, column 3, lines 44-46).

Regarding claim 8, which inherits the limitations of claim 6, Lindquist et al. discloses a reset input for receiving a reset signal that resets both the first latch device and the second latch device (column 3, lines 28-31 and 58-61).

Regarding claims 21-24, the claimed method includes features that correspond with subject matter mentioned above in the rejection of claims 1-4 is applicable hereto, wherein de-asserting a signal is equivalent to resetting a signal.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 13-20 and 29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sumi (U.S. Patent No. 5, 729, 179) in view of Lindquist et al. (U.S. Patent 6, 198, 355).

Regarding claim 13, which inherits the limitations of claim 9, Sumi discloses all the limitations of claim 13 except that a single phase detector comprises a comparison circuit that compares a phase of the reference clock signal with a phase of a signal having a frequency that is twice that of the comparison signal.

However, Lindquist et al. discloses a single phase detector comprising a comparison circuit (Fig. 2, column 3, lines 33-67) that compares a phase of the reference clock signal with a phase of a signal having a frequency that is twice that of the comparison signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the PLL of Sumi with the phase detector of Lindquist et al. since Lindquist et al. states that a phase detector which can compare a phase of the reference clock signal with a phase of a

signal having a frequency that is twice that of the comparison signal can lower the division ratio and reduce the noise contribution from the phase detector (Abstract).

Regarding claims 14-20, the claimed device includes features that correspond with subject matter mentioned above in the rejection of claims 2-8 is applicable hereto.

Regarding claim 29, which inherits the limitation of claim 28 (see rejection above) the claimed method includes features that correspond with subject matter mentioned above in the rejection of claim 13 is applicable hereto.

Regarding claims 30-32, the claimed method includes features that correspond with subject matter mentioned above in the rejection of claims 2-4 is applicable hereto.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 703-305-4097. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Curtis Odom
July 9, 2003

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600